Experiment

IPhO 2018
Lisbon, Portugal

Q1-1

English (Official)

Paper transistor (10 points)

Electronic technology in modern society is based on a simple, yet powerful device: the transistor, which can be used both as a switch and as an amplifier. The switch mode is used for storage and processing of digital information.

Here we will analyse two types of Field Effect Transistors (FET): JFET (Junction Field Effect Transistor) and the TFT (Thin Film Transistor).

We shall briefly explain here how a FET works. A FET is a non-linear 3 terminal device (the terminals being named Gate: G; Source: S; and Drain: D) that can control the current flow between Source and Drain by acting upon the voltage applied between the Gate and the Source. In a simple, although imperfect analogy, a FET works similarly to a water tap, the knob acting as the Gate controlling the water flow.

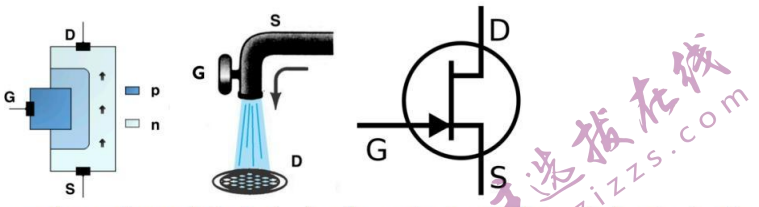

Figure 1. Scheme of an n-channel JFET (left), its hydraulic analogy (middle) and electric circuit symbol (right). The arrows in the JFET scheme indicate the flow of the electric current between Source (S) and Drain (D) through the narrow n-channel. The width of the channel depends on the applied voltage between the Gate (G) and the Source (S).

The Junction-FET (JFET) relies upon the properties of the junction between two types of a semiconducting material, such as p and n doped silicon, hence its name. A JFET has a narrow channel through which the current flows between Source and Drain, and in a n-channel FET this channel is made of n-type material. The width of such channel can be controlled in a precise way by applying a **negative** voltage between the Gate and the Source, $V_{GS} = V_G - V_S$. For a fixed V_{GS}, the current flowing between Source and Drain depends non-linearly on the applied voltage between Drain and Source, $V_{DS} = V_D - V_S$. For small V_{DS} voltages, however, the current does depend linearly on the applied voltage, thus the JFET displays ohmic behaviour. The output resistance, $R_{DS} = V_{DS}/I_{DS}$, however, does depend strongly on the applied V_{GS} voltage, closely following the law:

$$R_{DS} = \frac{R_{DS}^0}{1 - V_{GS}/V_P}, \tag{1}$$

where R_{DS}^0 is the output resistance at $V_{GS} = 0$ and $V_P < 0$ is a JFET parameter called the *pinch-off voltage*. Clearly, at the pinch-off voltage, the FET blocks current flow.

For any fixed $V_{GS} > V_P$, the current between Source and Drain will start to depart from the linear behaviour as we increase V_{DS}, and will at some point saturate at an almost constant value. Let I_{DSS} be the saturation current when $V_{GS} = 0$. In the saturation regime (large applied V_{DS}), the saturation current will depend on V_{GS} in the following way:

$$I_{DS} = I_{DSS}\,(1 - V_{GS}/V_P)^2\,. \tag{2}$$

Experiment

IPhO 2018
Lisbon, Portugal

Q1-2

English (Official)

We should stress two very important characteristics of a JFET. Although its voltage controlled output resistance can be quite low, the input resistance ($R_{GS} = V_{GS}/I_{GS}$) is extremely high, typically larger than $10^9\ \Omega$, so this device uses very little input current. Also, the capacitance of a small JFET is quite low making it a very fast device than can 'open and close' beyond MHz rates.

We now proceed to describe how a different type of FET, the TFT, works.

As any other FET, the TFT permits the control of a current between two contacts, the Drain and Source electrodes, by means of an applied potential at the third electrode, the Gate.

The Gate electrode is physically separated from the semiconductor layer by a dielectric that allows for the establishment of a vertical electrical field that will control the free charge carriers existing in the semiconductor (field effect). The dielectric layer can be replaced by an electrolytic membrane such as paper where mobile ions exist (see Figure 2) and in this case the voltage applied at the Gate will push ions with opposite charge to the semiconductor interface, creating a sheet of ionic charges that will modulate the free carriers' density existing within the semiconductor (Electrolyte Gated Transistors - EGTs). Researchers at Universidade Nova, Lisbon, were pioneers in developing in 2008 the "paper transistor", and are world leaders in this field.

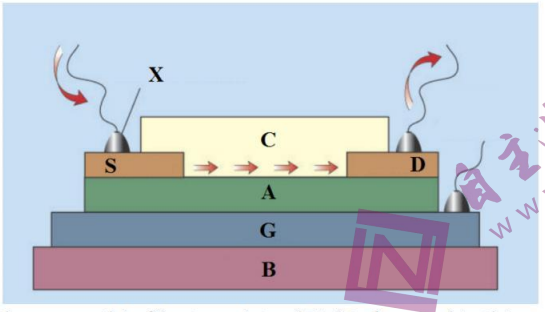

Figure 2. Scheme of the paper thin film transistor (TFT) to be used in this problem. S - Source; D - Drain; G - Gate; A - paper (dielectric); B - substrate; C - semiconductor layer (Gallium-Indium-Zinc oxide (GIZO)); X - Metal contacts. The arrows indicate the conventional current flow.

Similarly to JFETs, TFT transistors can operate in two fundamental operation modes, a linear mode and a saturation mode. In contrast to JFET, TFT intrinsic capacitance is a relevant parameter for the device performance.

In this experimental problem you will examine how an n-channel JFET and a paper TFT work.

You will determine the Characteristic Curves (CCs) of these devices by measuring the current between S and D (I_{DS}) through the application of distinct voltages at G (V_{GS}) and D (V_{DS}).

The two most important CCs are the output and the transfer curves:

- **Output Curve**: For this curve the current between Source and Drain (I_{DS}) will be measured and plotted as a function of the voltage between Source and Drain (V_{DS}), with V_{DS} swept from 0 V up to $+3$ V , in steps, while keeping V_{GS} constant.
- **Transfer Curve:** For this curve I_{DS} will be measured and plotted against V_{GS}. V_{DS} will be kept constant at a suitable value for the transistor to work in the **saturation mode** and V_{GS} will be swept in steps from -3 to 0 V.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-3

English (Official)

Equipment

The following set of equipment (Figure 3) is provided for this experimental problem:

1. multimeter
2. JFET transistor (provided inside a labelled plastic bag)
3. cables (10) with alligator clips
4. flat alligator clips (4, provided inside a plastic bag)
5. battery pack (4×1.5 V)
6. battery holder
7. mini-breadboard with support
8. jumper wires (3) to connect to the mini-breadboard
9. HB pencil
10. silver ink conductive pen (Circuit Scribe)
11. chronometer
12. sheet of paper with printed circuits and an embedded TFT that uses paper as dielectric layer (Figure 4)
13. bag with writing material (1 pen, 1 pencil, 1 eraser/sharpener, 1 ruler)

Experiment

IPhO 2018
Lisbon, Portugal

Q1-4

English (Official)

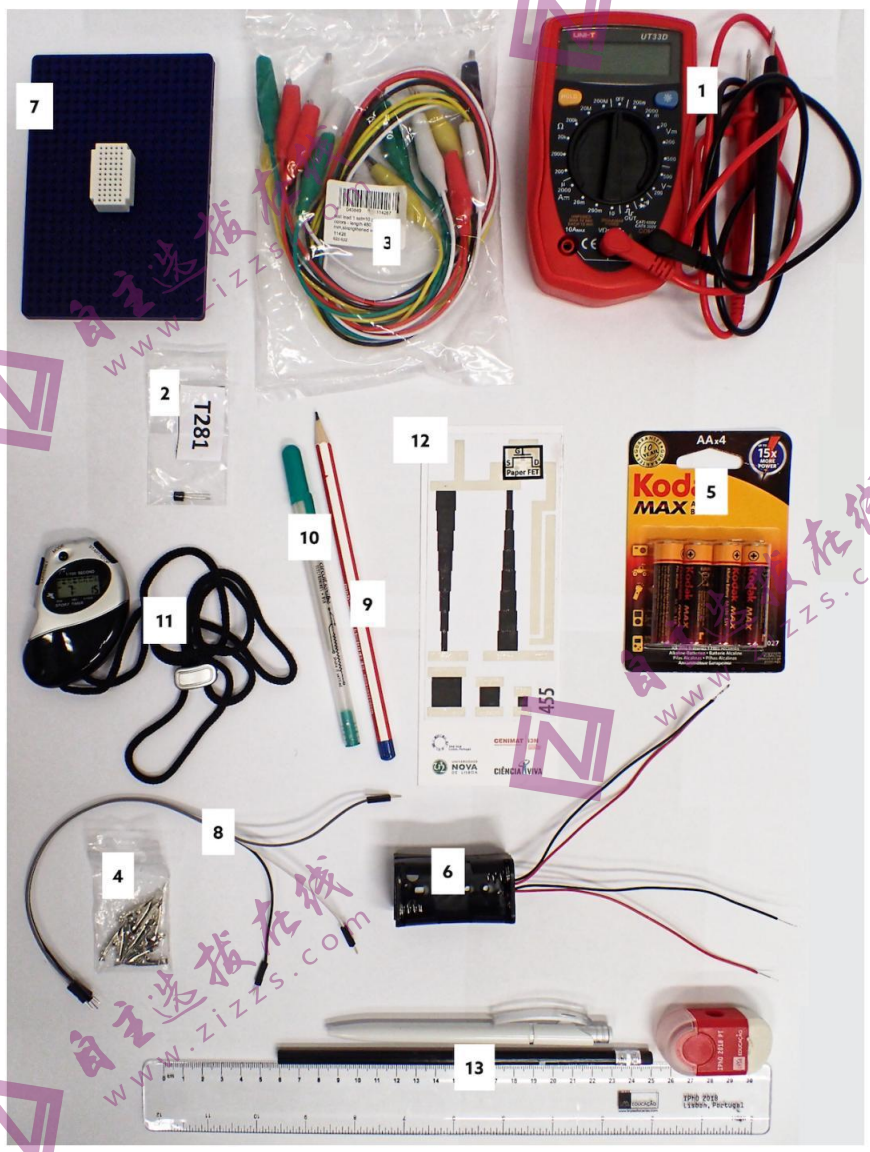

Figure 3. Equipment set.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-5

English (Official)

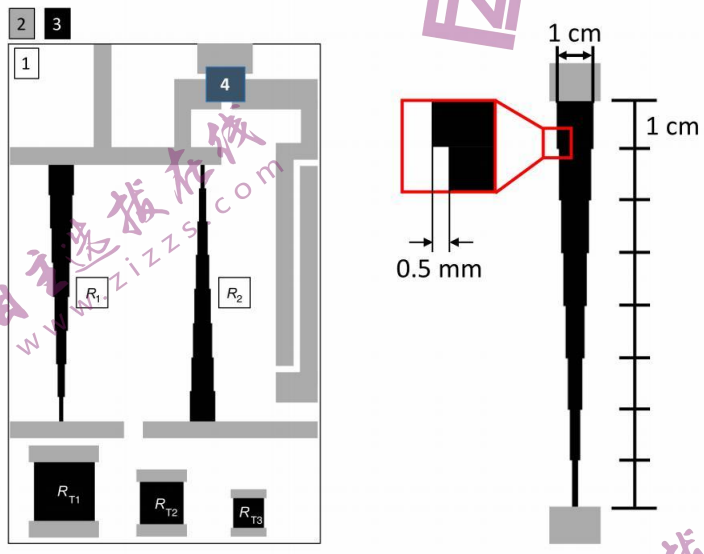

Figure 4. Left: Sheet of paper with printed circuits included in the equipment: paper (1) , silver conductive tracks (2), carbon resistive tracks (3), paper transistor (4), voltage divider resistances (R_1 and R_2). Right: Physical dimensions of the voltage divider resistances (the steps of 0.5 mm are constant for each segment).

Important precaution:
Do not fold the sheet of paper with the printed circuits and embedded transistor as this will easily damage it. Try to leave it as flat as possible during measurements in order to reach best results.

For the measurements it is important to take into account the following **important information**:

Experiment

IPhO 2018
Lisbon, Portugal

Q1-6

English (Official)

- The multimeter should always be operated in **DC mode**.
- The multimeter does not autorange and you should carefully choose the most appropriate ranges for your measurements. In case a overflow occurs the display will show either "1" or "-1" (left justified on the display), for positive and negative values, respectively, and you should change to a lower range.
- The low-current ranges are protected by a 315 mA fuse. **Avoid by all means to create a short circuit** between the battery and the multimeter because a high current will blow up the fuse!
- The internal resistance of the multimeter when operating in voltmeter mode is $10\,\mathrm{M\Omega}$.
- When operating as ammeter, the internal resistance of the multimeter depends on the range as shown in the following table:

Range	R_{int}/Ω
200 mA	1.0
20 mA	10
2 mA	100

Table 1. Internal resistance of the provided multimeter when operated as ammeter.

Thus, when the multimeter is being used in DC ammeter mode, there will be a voltage drop up to 200 mV between its terminals at full scale when operated in any of the 3 available DC ranges.

Part A. Circuit dimensioning (2.5 points)

To achieve the necessary V_{DS} and V_{GS} voltages you will use two carbon resistors printed on paper(R_1 and R_2, see Fig. 4) and voltage divider circuitry to dimension the circuit for the right potential drops. R_1 and R_2 will be the total resistance (R_{tot}) of a voltage divider circuit. When applying a constant voltage (in this case about 3 V from the battery) across R_1, for instance, we will see a voltage drop along it from 3 V (V_{in}, the positive contact of the battery) to ground (0 V; from now on, we designate as ground the common contact of the two battery packs). R_{tot} can be divided into essentially two resistances (R_{x} and R_{y}) to achieve the desirable V_{out} (Figure 5).

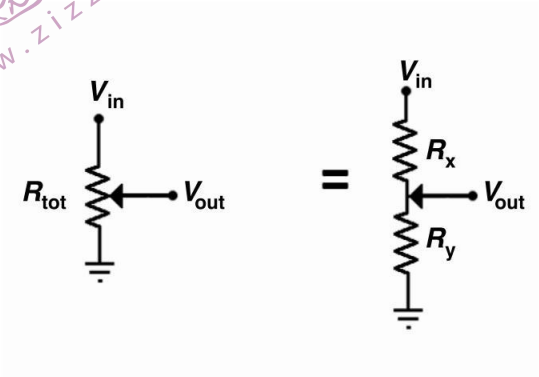

Figure 5. Voltage divider circuit.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-7

English (Official)

A.1	Write down the expression for the output voltage, V_{out}, as a function of V_{in} and resistances R_x and R_y.	0.2pt
A.2	Measure the resistance of the three test resistors on the bottom part of the sheet (R_{T1}, R_{T2} and R_{T3}) with the multimeter. Carry out enough measurements with different positions on the silver contacts. Enter the values in the Answer Sheet. Calculate the average value and estimate the uncertainty for the resistance of each test resistor.	0.5pt
A.3	Show that the resistance of a square thin film with a certain resistivity, ρ, should be independent of the length of its side. This size-independent resistance is called *sheet resistance* and is denoted $R_\square$.	0.3pt
A.4	Calculate the average value of the sheet resistance of the carbon film from the data in A.2 and obtain the resistivity, ρ, of the carbon film with an estimation of its uncertainty (consider a thickness t of the carbon film of 20 ± 1 μm).	0.4pt
A.5	Show that the theoretical value of the R_1 and R_2 resistances is $R_1 = R_2 = \kappa R_\square$, $\kappa \sim 14.2897$. Measure R_1 and R_2 and write down the values in the Answer Sheet. Determine the experimental value of κ and compare it with the theoretical value.	0.5pt

Using the provided silver ink pen, draw 7 equally spaced conductive lines along each of the provided resistors (as exemplified in Figure 6). These individual lines will serve as the contact points for the voltage dividers.

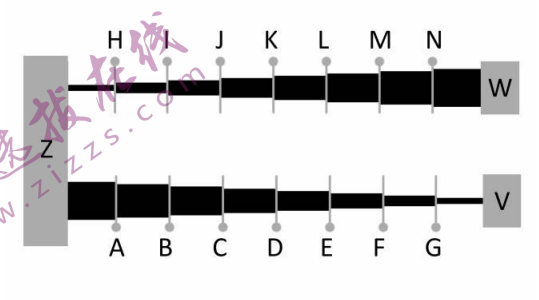

Figure 6. Line drawing example and naming scheme of the contact points.

A.6	Measure the resistances R_x and R_y for all contact points. R_x is defined as the resistance between the contact point and points V (resistor 1) or W (resistor 2), and R_y is defined as the resistance between the contact point and point Z. Fill the provided tables in the Answer Sheet.	0.3pt

Insert the 4 AA batteries in the battery holder. Please observe carefully the correct battery polarity and

Experiment

IPhO 2018
Lisbon, Portugal

Q1-8

English (Official)

make sure you do not produce a short circuit. Then, physically connect the battery pack as depicted in Figure 7. Make sure you do not damage the silver tracks with the alligator clips.

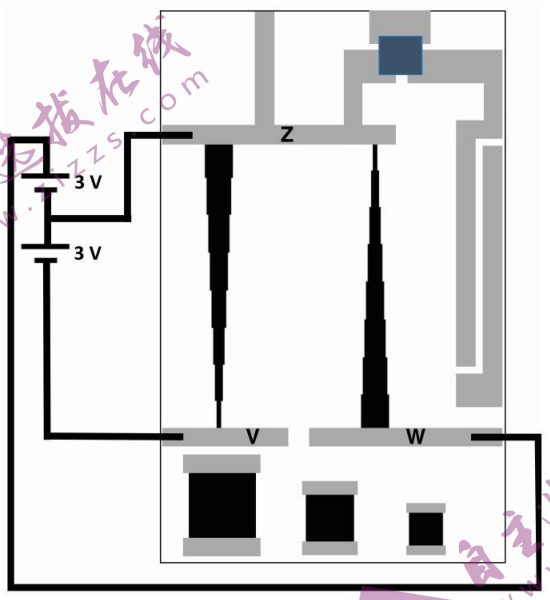

Figure 7. Battery connections

A.7	Measure V_{out} at each contact point, V_{out} being the voltage measured with respect to point Z and enter the values in the provided tables in the Answer Sheet.	0.3pt

This concludes the circuit dimensioning part and you can now proceed to measure the CCs of the JFET transistor.

Part B. Characteristic Curves of the commercial JFET transistor (4.5 points)

In order to characterise the JFET transistor you will use the setup depicted in Figure 8. Start by identifying the three contacts (S, D and G) on the provided JFET transistor - **pay attention to the correct identification of the contacts, as the device is not symmetric!** You may use the provided minibreadboard with support to mount the JFET transistor. The provided jumper wires are to be used with the mini-breadboard.

Using the provided cables, connect the Gate and the Source of the transistor to ground (point Z of the circuit, at 0 V). Throughout this part of the problem, the Source of the JFET should always be kept connected to ground.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-9

English (Official)

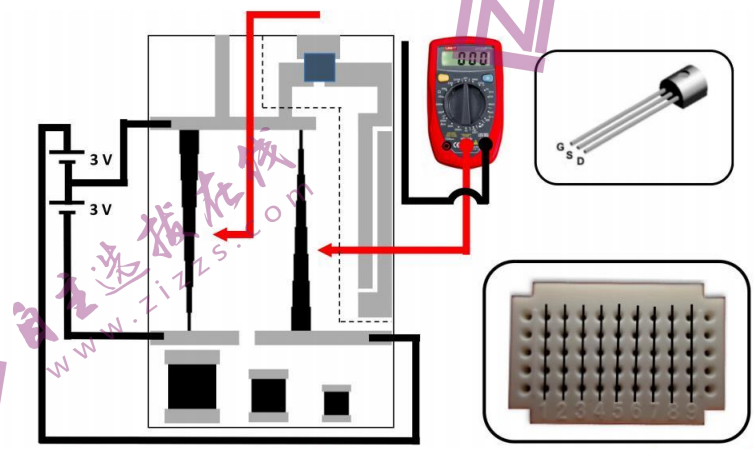

Figure 8. Setup for the determination of the JFET characteristic curves. The part of the circuit inside the dashed region that includes the TFT is not to be used in part B of the problem. The top inset shows how to identify the Gate, Source and Drain of the JFET transistor. The bottom inset shows how the holes of the mini-breadboard are connected. All holes in a numbered column are internally interconnected and isolated from the holes of other columns. The picture of the multimeter is merely illustrative: you are in charge of selecting the appropriate measuring mode and range in the rotary selector of the multimeter.

B.1	Connect the gate of the transistor to ground ($V_{GS} = 0$). Then connect one of the cables of the multimeter, that should be used in DC current mode, to the drain of the transistor and with the other cable touch the point with the highest voltage available in the voltage dividers. Write down in the answer sheet the value of the current I_{DS}.	0.2pt

B.2	Measure the current I_{DS} for different positive voltages applied to the Drain, while keeping $V_{GS} = 0$. Then change the circuit to apply a negative voltage between the Gate and the Source of the transistor ($V_{GS} < 0$) and repeat the measurements of I_{DS} as a function of the positive applied voltage between Drain and Source. Fill with your values the tables provided in the Answer Sheet.	0.8pt

When the voltage divider circuit is connected to a low resistance load (Figure 9), the voltage values provided by the voltage divider, V_{out}^{L}, are different from the nominal values V_{out} measured when the load is a high resistance, such as the case of a high impedance voltmeter.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-10

English (Official)

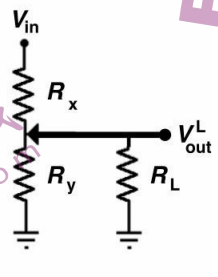

Figure 9. Voltage divider with a load.

B.3	Consider that the voltage divider is connected to a load R_L. Obtain an expression for the correction factor $f = V_{out}^L/V_{out}$ as a function of R_L, R_x and R_y.	0.2pt

The JFET transistor has a low output resistance when $V_{GS} = 0$, namely $R_{DS}^0 \sim 50\ \Omega$. However, this resistance increases significantly when the Gate is polarised negatively with respect to the Source. For $V_{GS} < 0$ the output resistance follows closely the law given by equation (1).

B.4	Using the appropriate correction factors, calculate V_{DS}, the voltage drop between Drain and Source, for all the points measured in B.2. Consider the following nominal data for the JFET used in this problem : $R_{DS}^0 = 50\ \Omega$, $V_P = -1.4$ V.	1.2pt
B.5	Plot the output curves $I_{DS}(V_{DS})$ for your JFET transistor.	0.5pt
B.6	Consider the transistor in operation at small V_{DS}. Obtain the *experimental* values of R_{DS} of your JFET for different V_{GS} and plot the data.	0.5pt
B.7	Plot the transfer curve $I_{DS}(V_{GS})$ of your JFET transistor for $V_{DS} \sim +3$ V.	0.3pt

When the JFET transistor is in saturation mode, the current I_{DS} follows closely the law expressed by equation (2).

B.8	From the measured data, obtain I_{DSS} and the *pinch-off* voltage, V_P, for your device. Compare the value obtained of V_P with the nominal value.	0.4pt

An important parameter of a JFET transistor, in particular when it is used in amplifiers, is the so called transistor transconductance, g, defined as

$$g = \frac{\partial I_{DS}}{\partial V_{GS}}. \tag{3}$$

For a function of two variables $f(x, y)$, the notation $\frac{\partial f}{\partial x}$ means the derivative of f with respect to x when y is kept constant.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-11

English (Official)

B.9	Obtain, from the measured transfer curve, the transconductance of your device for $V_{GS} = -0.50$ V. Compare it with the calculated value obtained from the model equation (2).	0.4pt

Part C. The Paper Thin Film Transistor (2.0 points)

From now on, you discard the JFET, and all following tasks and questions relate to the paper thin film transistor (TFT) located in the upper corner of the printed circuit. The TFT Gate, Source and Drain are marked in Figure 10. Connect the TFT Gate and the Source to ground. Also in this part of the problem the Source of the paper TFT should always be connected to the common contact of the battery packs, i.e. 0 V, as shown in Figure 10. Polarise the transistor with $V_{DS} > 0$, via one of the voltage circuit dividers (Figure 10). Check that a current is flowing through the ammeter.

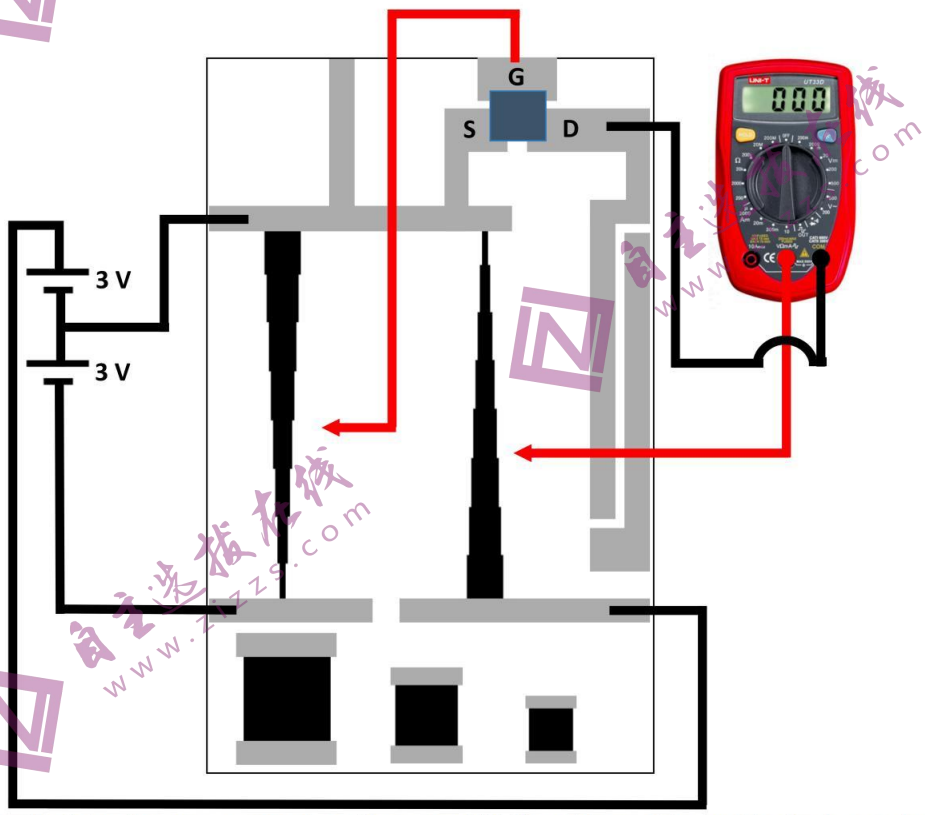

Figure 10. Setup for measurements on the paper TFT. The picture of the multimeter is merely illustrative: you are in charge of selecting the appropriate measuring mode and range in the rotary selector of the multimeter.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-12

English (Official)

C.1	Apply $V_{DS} = +3.0$ V. Close the transistor by applying $V_{GS} = -3.0$ V. Wait for 1 min so that the the transistor closes. Write down in the answer sheet the residual value of the current, I_{closed} . Then open the transistor by putting $V_{GS} = 0$, while keeping $V_{DS} = +3.0$ V. Measure the current as function of time, starting at the instant when you open the transistor, for at least 5 min and collect the data $I_{DS}(t)$ in the answer sheet.	0.8pt
C.2	Plot $I_{DS}(t)$. There is a superposition of two exponential processes in the time dependence, one with a much larger time constant (τ_2) than the other (τ_1). Determine the shorter time constant, τ_1.	1.2pt

Part D. Inverter circuit (1.0 points)

In microelectronic circuitry one of the most important circuits is the inverter, that is able to invert a digital input. For instance if V_{in} = high then V_{out} = low and vice-versa. A transistor is once again at the basis of the circuit and one of the simplest designs is the so called common source amplifier, depicted in Figure 11, using a transistor and a load resistance (R_L). In this case $V_{in} = V_{GS}$ and V_{out} is the voltage measured at the Drain electrode of the transistor. Thus, in this part we will monitor what happens to V_{out} while sweeping V_{GS} from -3 V to 0 V.

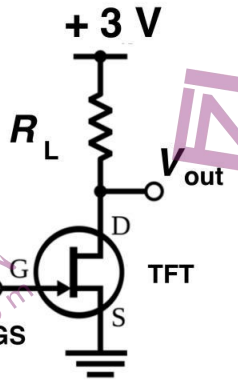

Figure 11. Common source amplifier and inverter circuit.

In the setup of Figure 11 the transistor is the paper TFT and R_L is a load resistance you are going to add now, manually, by connecting the Drain contact of the transistor with the V_{in} contact using a pencil track, as indicated in Figure 12. While you write, you are actually depositing thin layers of conductive graphite on the paper so the more layers you draw on top of each other, the lower the resistance will get. While drawing R_L make sure to continuously monitor its resistance. To pull V_{out} as close to 0 V as possible the load resistance should be large enough. So, while drawing the resistance, aim for a value close to the target value $R_L = 200$ kΩ .

You can either use the pencil to decrease R_L or the eraser to increase it. You should aim to obtain a value differing not more than 10% from the aimed value.

Experiment

IPhO 2018
Lisbon, Portugal

Q1-13

English (Official)

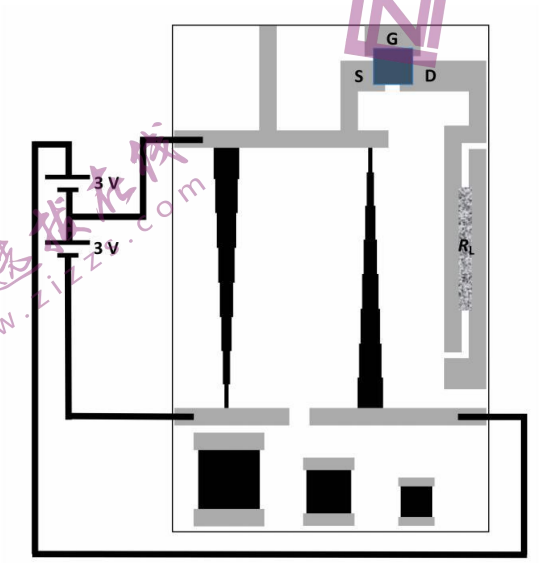

Figure 12. Setup for the inverter/common source amplifier configuration.

Use the included HB pencil and draw by hand a carbon resistor with value of $R_L \simeq 200\ \mathrm{k\Omega}$ to be used as a load resistor of the paper TFT to build the inverter circuit (see Figure 12).

D.1	Write down in the Answer Sheet the measured R_L value you have reached. Setup the inverter circuit (Figure 12) using the carbon track resistor and the paper TFT. Before the measurement, remember that you should turn the transistor fully off by applying $V_{GS} = -3$ V and wait for ~ 1min . Then measure V_{out} as you sweep V_{GS} from -3 V to 0 V and take readings of V_{out} with a stabilization time for each point up to a maximum of 100 s . Enter the measured values in the Answer Sheet.	0.5pt
D.2	Plot the measured $V_{out}(V_{in})$ voltage transfer curve and draw a smooth trend curve through the data points.	0.5pt

关于我们

自主选拔在线是致力于提供新高考生涯规划、强基计划、综合评价、三位一体、学科竞赛等政策资讯的升学服务平台。总部坐落于北京，旗下拥有网站（**网址：www.zizzs.com**）和微信公众平台等媒体矩阵，用户群体涵盖全国90%以上的重点中学师生及家长，在全国新高考、自主选拔领域首屈一指。

如需第一时间获取相关资讯及备考指南，请关注**自主选拔在线**官方微信号：**zizzsw**。